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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,505	04/09/2004	Steve C. Huang	ID-04-01	9848

30349 7590 01/23/2006

JACKSON & CO., LLP
6114 LA SALLE AVENUE
SUITE 507
OAKLAND, CA 94611-2802

EXAMINER

LIN, SUN J

ART UNIT	PAPER NUMBER
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2825

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/821,505

Applicant(s)

HUANG ET AL.

Examiner

Sun J. Lin

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 April 2004.
2a) ☐ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☒ Claim(s) 1-30 is/are allowed.
6) ☐ Claim(s) _____ is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 8/30/2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 04/27/05.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/821,505 filed on 04/09/2004.
Claims 1 – 30 remain pending in the application.

Quayle Action

2. This application is in condition for allowance except for the following formal matters:

Specification Objections

Page 32, line 5, before "one or more" delete ~~the~~.

Page 32, line 5, after "one or more" insert ~~the partitioned~~.

Page 32, line 10, change "Scan cell" to ~~The scan cell~~.

Page 32, line 11, before "gate-level netlist" insert ~~a~~.

Drawing Objections

Replace draft drawings (Figure 4, Figure 5, Figure 7, Figure 8, Figure 9, Figure 10A, and Figure 12) with official ones.

Figure 10B, attach "arrow" at end of each line to indicate flow direction of the flow chart.

Claim Objections

Claim 1, line 2, before "steps" delete ~~the~~.

Claim 1, line 3, change "an integrated circuit" to ~~the integrated circuit~~.

Claim 1, line 5, before "one or more" delete ~~the~~.

Claim 1, line 5, after "one or more" insert ~~the partitioned~~.

Claim 1, line 5, before "multi-cycle" insert ~~the~~.

Claim 1, line 8, change "set of constraint setting" to ~~constraint setting set~~.

Claim 1, line 9, before "design" insert ~~the~~.

Claim 2, line 1, before "process" insert ~~computer implemented~~.

Claim 3, line 1, before "process" insert ~~computer implemented~~.

Claim 4, line 1, before "process" insert ~~computer implemented~~.

Claim 4, line 5, change "the block" to ~~the logic block~~.

Claim 4, line 8, after "other" to ~~logic~~.

- Claim 4, line 10, before "design partition" insert **—the—**.
- Claim 5, line 1, before "process" insert **—computer implemented—**.
- Claim 6, line 1, before "process" insert **—computer implemented—**.
- Claim 6, line 2, before "affected" delete **—the—**.
- Claim 7, line 1, before "process" insert **—computer implemented—**.
- Claim 8, line 1, before "process" insert **—computer implemented—**.
- Claim 8, line 1, change "the step" to **—a step—**.
- Claim 8, line 3, change "setup" to **—initial setup sequence—**.
- Claim 9, line 2, before "steps" delete **—the—**.
- Claim 9, line 5, before "scan cell" insert **—corresponding—**.
- Claim 9, line 6, before "scan cell" insert **—corresponding—**.
- Claim 10, line 1, before "process" insert **—computer implemented—**.
- Claim 10, line 3 – 4, before "scan cell" insert **—corresponding—**.
- Claim 11, line 1, before "process" insert **—computer implemented—**.
- Claim 11, line 1, change "the scan cell" to **—the corresponding scan cell—**.
- Claim 11, line 2, change "corresponds the dual scan cell" to **—the dual scan cell corresponds—**.
- Claim 12, line 2, before "steps" delete **—the—**.
- Claim 12, line 3, before "gate-level netlist" insert **—a—**.
- Claim 12, line 6, change "one or more cells" to **—one or more of the cells—**.
- Claim 12, line 6, before "corresponding" delete **—a—**.
- Claim 13, line 1, before "process" insert **—computer implemented—**.
- Claim 13, line 1, change "the target characteristics" to **—target characteristics of the closest target characteristics—**.
- Claim 14, line 1, before "process" insert **—computer implemented—**.
- Claim 14, line 1, change "the target characteristics" to **—target characteristics of the closest target characteristics—**.
- Claim 15, line 1, before "process" insert **—computer implemented—**.
- Claim 15, line 1, change "timing" to **—target—**.
- Claim 16, line 1, before "process" insert **—computer implemented—**.
- Claim 16, line 2, change "the scan cell" to **—a scan cell—**.
- Claim 16, line 2, change "the corresponding cell" to **—a corresponding cell—**.
- Claim 17, line 1, before "process" insert **—computer implemented—**.
- Claim 17, line 2, before "the context delay" insert **—wherein—**.

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- Claim 18, line 1, before "process" insert **—computer implemented—**.
- Claim 19, line 1, before "process" insert **—computer implemented—**.
- Claim 20, line 2, before "steps" delete **—the—**.
- Claim 20, line 3, change "an integrated circuit" to **—the integrated circuit—**.
- Claim 20, line 8, change "set of constraint setting" to **—constraint setting set—**.
- Claim 21, line 1, before "process" insert **—computer implemented—**.
- Claim 21, line 2, after "setting" insert **—set—**.
- Claim 22, line 1, before "process" insert **—computer implemented—**.
- Claim 22, line 2, before "steps" delete **—the—**.
- Claim 22, line 3, before "gate-level netlist" insert **—a—**.
- Claim 22, line 6, change "one or more cells" to **—one or more of the cells—**.
- Claim 23, line 1, before "process" insert **—computer implemented—**.
- Claim 23, line 1, change "the target characteristics" to **—target characteristics of the closest target characteristics—**.
- Claim 24, line 1, before "process" insert **—computer implemented—**.
- Claim 24, line 1, change "the target characteristics" to **—target characteristics of the closest target characteristics—**.
- Claim 25, line 1, before "process" insert **—computer implemented—**.
- Claim 25, line 5, change "the block" to **—the logic block—**.
- Claim 25, line 8, change "other blocks" to **—other logic blocks—**.
- Claim 25, line 10, before "design partition" insert **—the—**.
- Claim 26, line 1, before "process" insert **—computer implemented—**.
- Claim 27, line 1, before "process" insert **—computer implemented—**.
- Claim 27, line 1, change "the step" to **—a step—**.
- Claim 27, line 3, change "setup" to **—initial setup sequence—**.
- Claim 28, line 6, before "one or more" delete **—the—**.
- Claim 28, line 6, after "one or more" insert **—the partitioned—**.
- Claim 28, line 6, before "multi-cycle" insert **—the—**.
- Claim 28, line 9, change "set of constraint setting" to **—constraint setting set—**.
- Claim 29, line 1 – 2, change "The process of claim 19 wherein...setting se include:" to **—The computer program product of Claim 28, wherein the computer program code adapted to select and to apply the constraint setting is further adapted to:—**.
- Claim 29, line 3, change "extracting" to **—extract—**.

Claim 29, line 4, change "applying" to **—apply—**.

Appropriate corrections are required.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

Reasons for Allowance

3. The following is an examiner's statement of reasons for allowance:

Claims 1 – 30 are allowed because the prior art does not teach or suggest the following subject matter:

- A computer implemented process of performing design of testability analysis and synthesis in an integrated circuit design, comprising steps of partitioning each logic block in the integrated circuit design based on one or more boundaries of multi-cycle initial setup sequence and excluding one or more of the partitioned logic blocks with multi-cycle initial setup sequence from valid candidate blocks in combination with other limitations as recited in independent **Claim 1** and **Claim 20**, respectively;
- A computer implemented process for performing class and cell selection procedure in *scan cell replacement* for an integrated circuit design, comprising a steps of, based on a cost function, establishing an affinity between a cell and a corresponding scan cell which will replace it in combination with other limitations as recited in independent **Claim 9**;
- A computer implemented process of performing scan cell replacement for an integrated circuit design, comprising a step of replacing one or more of cells with corresponding one or more scan cells having the closest target characteristics in combination with other limitations as recited in independent **Claim 12**;
- A computer program product, comprising computer program code adapted to partition each logic block in the integrated circuit design based on one or more boundaries of multi-cycle initial setup sequence and exclude one or more of the partitioned logic blocks with multi-cycle initial setup sequence

from valid candidate blocks in combination with other limitations as recited in independent **Claim 28**.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 10:00AM - 7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Jack Chiang* can be reached on (571) 272 - 7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun J. Lin
Primary Examiner
Art Unit 2825
January 17, 2006

